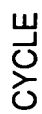


PRIOR ART

FIG. 3



420

[illegible]

422

PRIOR ART

FIG. 4

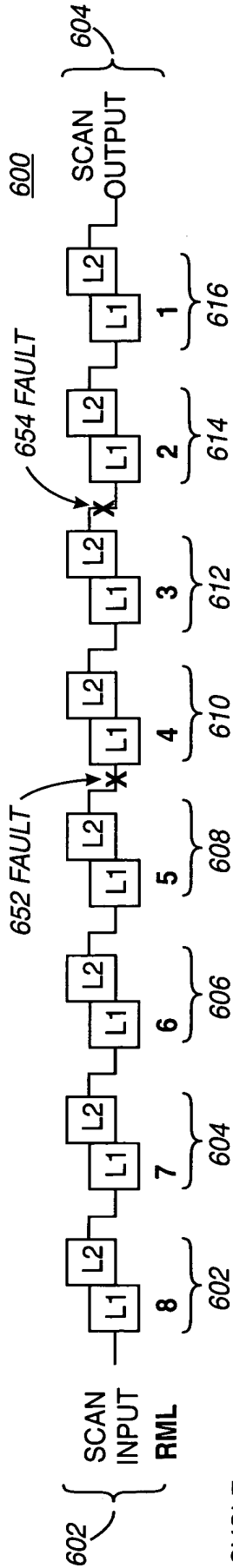


520

522

FIG. 5

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LOAD ALL
ZERO'S IN
FAILING
REGION

?	?	?	?	?	?	?	?	?
0	?	?	?	?	?	?	?	?
0	0	?	?	?	?	?	?	?
0	0	0	?	?	?	?	?	?
0	0	0	0	?	?	?	?	?
0	0	0	0	0	?	?	?	?
0	0	0	0	0	0	?	?	?
0	0	0	0	0	0	0	?	?
0	0	0	0	0	0	0	0	?
0	0	0	0	0	0	0	0	0

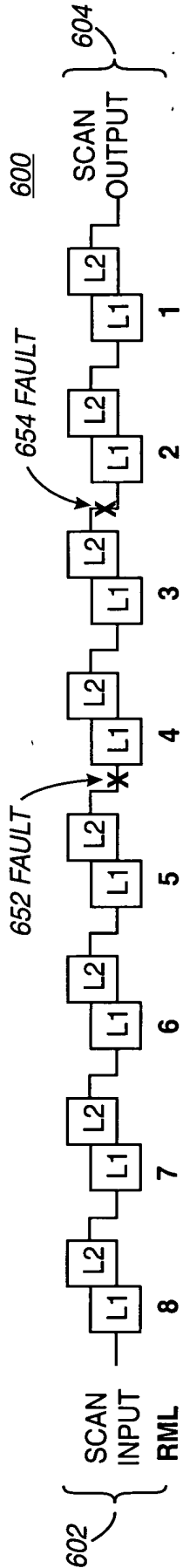
UNLOAD IN
OPERATING
REGION

0	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	1	0
0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	1	1	1
0	0	0	0	0	1	1	1	1

PRIOR ART

FIG. 6

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CYCLE

LOAD ALL
ZERO'S IN
FAILING
REGION

CYCLE	0	1	2	3	4	5	6	7	8
?	?	?	?	?	?	?	?	?	?
0	?	?	?	?	?	?	?	?	?
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0

720

CYCLE

UNLOAD IN
OPERATING
REGION

CYCLE	0	1	2	3	4	5	6	7
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0

722

PRIOR ART

FIG. 7

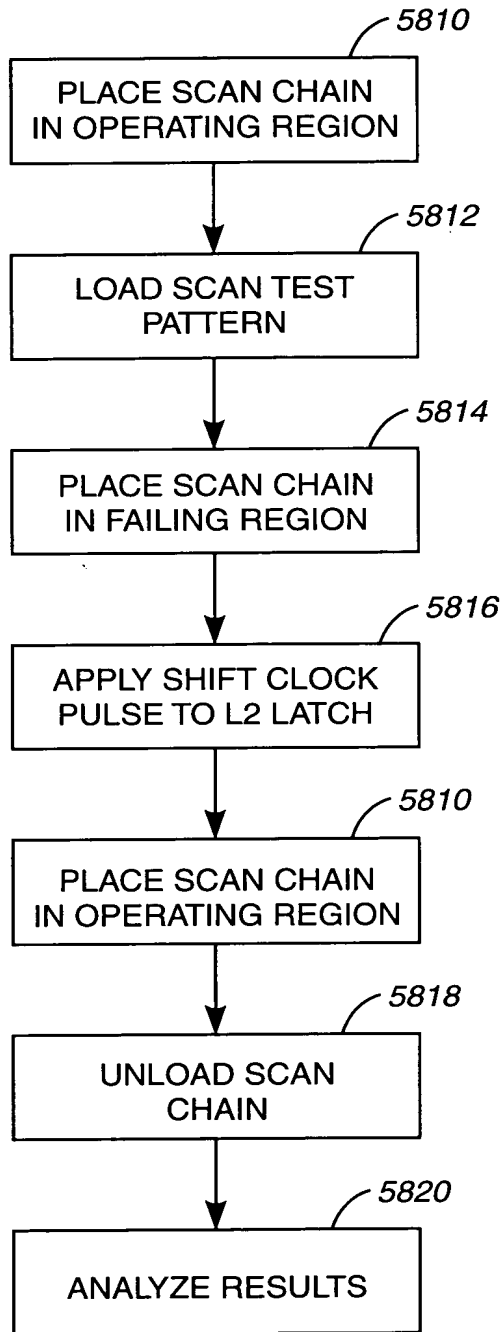


FIG. 8

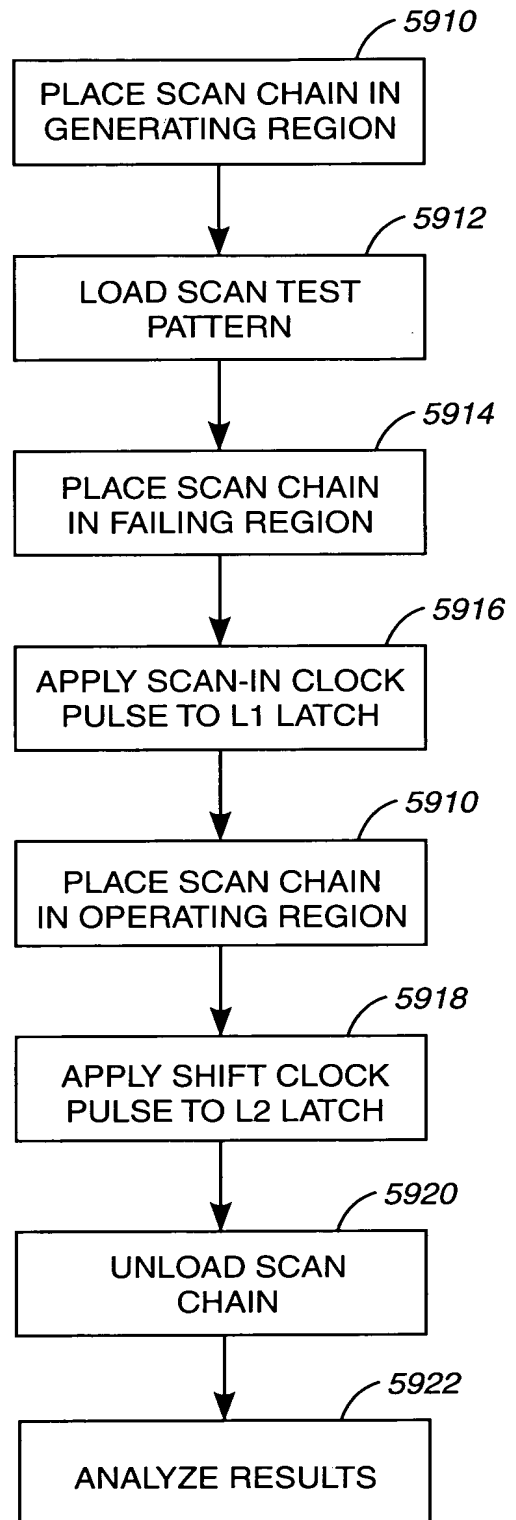
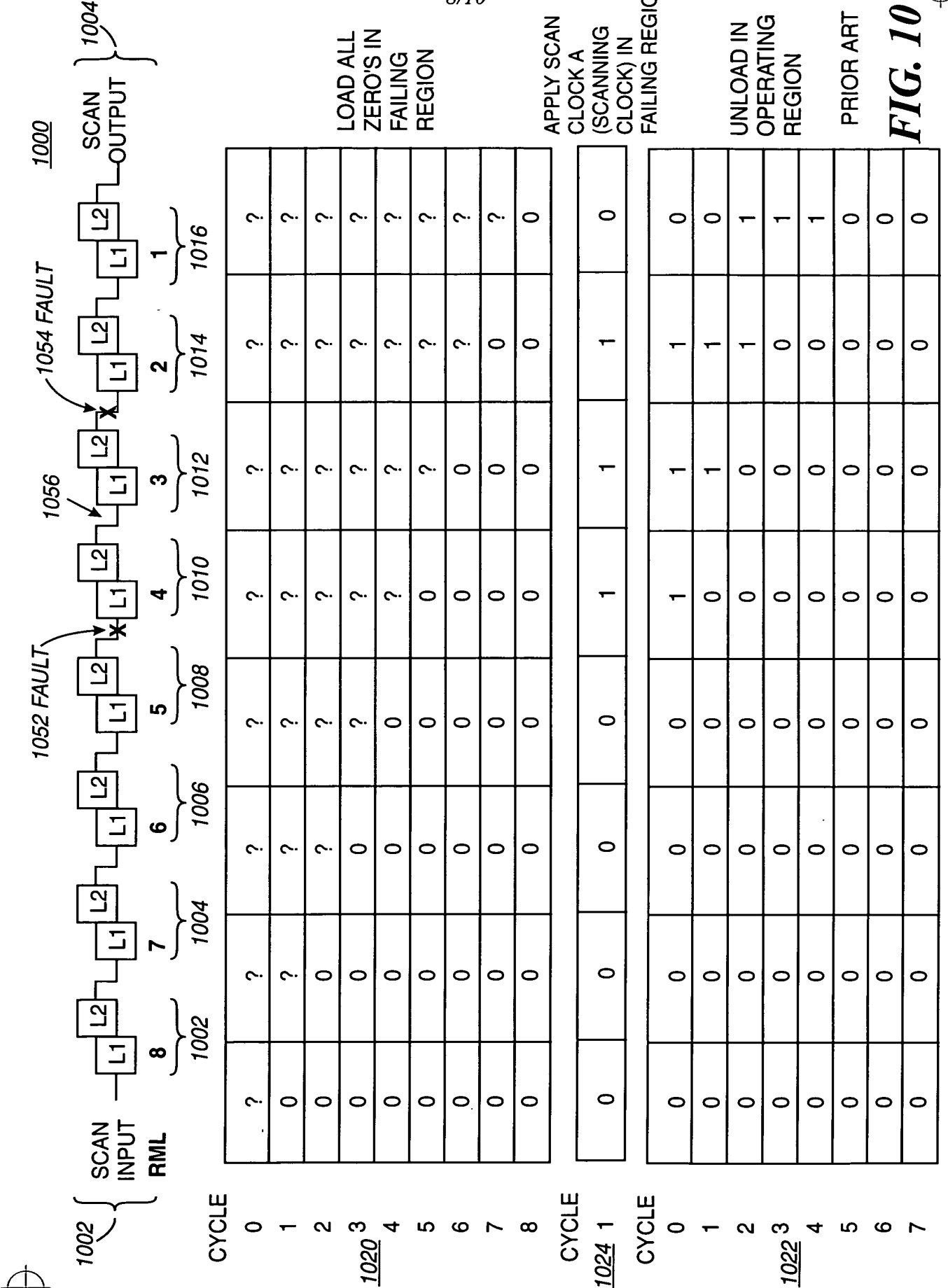


FIG. 9

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INPUT	1102 { RML8		1104 { RML7		1106 { RML6		1108 { RML5		1110 { RML4		1112 { RML3		1114 { RML2		1116 { RML1	
	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2
LOAD L1 AND L2 WITH ZEROS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SWITCH TO FAILING REGION	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0
CLOCK A	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0
SWITCH TO OPERATING REGION	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
CLOCK B	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0
UNLOAD L2		0		0		0		0		1		1		1		0

1120

1122

1124

1126

1128

1130

FIG. 11
1100

10/10

INPUT	1202		1204		1206		1208		1210		1212		1214		1216	
	RML8		RML7		RML6		RML5		RML4		RML3		RML2		RML1	
	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2	L1	L2
LOAD L1 AND L2 WITH ZERO'S	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SWITCH TO FAILING REGION	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0
CLOCK B	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0
SWITCH TO OPERATING REGION	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0
UNLOAD L2		0		0		0		1		1		1		0		0

1220

1222

1224

1226

1228

1200
FIG. 12